# Advanced VLSI Training on Xilinx FPGA's

<u>Agenda:</u>
**Day 1:**

- Introduction on VLSI Latest Advancements
- Xilinx FPGA's Architecture Overview (Artix to ZYNQ Ultra Scale Plus :: 45nm to 16nm ICs)
- **Lab : Xilinx Vivado Design Flow (Understanding all features)**
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bit-stream and verify in hardware.
- Introduction about the Nexys4DDR FPGA and Its target Applications
- **Lab : Create an Application and Implementing a Hardware Debugging using the IP Core**
  - Writing the Verilog code for own application
  - Utilizing IP catalog and Creating our Own Application, implementing the same on Hardware

**Day-2:**

 Introduction to Virtual Input Output Concepts

- **Lab : Application on VIO (how to use more number of I/Os:: Up-to 256 IOs with Nexys4DDR)**
  - Writing own code and configuring VIO in Vivado IP Cores
  - Adding the core into own source code
  - Implementing on the Hardware
- **Lab : Interfacing application**
  - Bluetooth interface on AV A7 board
  - TFT interface on AV A7 board

**Day-3:**

- **Lab : Application on Analog Signals**
  - Writing Application on Analog to Digital converters
  - Giving Analog input to the hardware and Verifying
- **Lab : Application Interfacing VGA**
  - Interfacing VGA
  - Analysis over the Die Temperature, Sensors

**Day-4:**

- Introduction to ZYNQ Families and Its Applications :: Zed Board
  - Interfacing the pmod wifi module by using the IP
  - Working on SDK with Pmod wifi

**Day-5:**

- **Pmod interfacing on Zed and Zybo**
  - Pmod OLEDrgb
  - Pmod COM3
  - Pmod JSTK2
  - Pmod seven segment display